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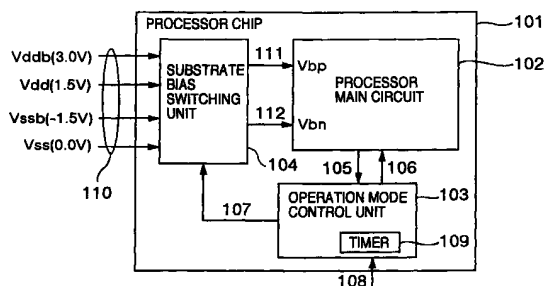 **Strehl Schübel-Hopf & Partner**
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(54)   **LOW-POWER PROCESSOR**

(57)   The feature of the present invention consists in: a processor main circuit for executing program instruction strings on a processor chip; a substrate bias switching unit for switching voltages of substrate biases applied to a substrate of the processor main circuit; and an operation mode control unit for controlling, in response to the execution of an instruction to proceed to a stand-by mode in the processor main circuit, the substrate bias switching unit in such a way that the biases are switched over to voltages for the stand-by mode, and for controlling, in response to an interruption of the stand-by release from the outside, the substrate bias switching unit in such a way that the biases are switched over to voltages for a normal mode, and also for releasing, after the bias voltages switched thereto have been stabilized, the stand-by of the processor main circuit to restart the operation.

FIG.1

EP 0 943 978 A1

Description

TECHNICAL FIELD

[0001]   The present invention relates to a semiconductor integrated circuit device such as a processor, and more particularly to a microprocessor which is capable of realizing the high speed operation as well as the low power consumption by controlling substrate biases of a processor circuitry constituted by MOS transistors in accordance with an operation mode of the processor.

[0002]   At the present time, for realization of a microprocessor, an integrated circuit employing CMOSs is widely used. The power consumption of the CMOS circuit is classified into the dynamic power consumption due to charge and discharge during the switching, and the static power consumption due to a leakage current. Out of them, since the dynamic power consumption is proportional to a power source voltage Vdd squared and hence occupies the large power consumption, in order to promote the low power consumption, it is effective to reduce the power source voltage. Then, in recent years, the power source voltages of many microprocessors have been reduced.

[0003]   As for the present low power consumption type microprocessor, there is known the microprocessor which includes the power management mechanism and which has a plurality of operation modes provided therein and in accordance therewith, stops the supply of a clock to execution units during the stand-by. By stopping the clock supply, the dynamic power consumption due to the switching in the unnecessary units can be reduced as much as possible. However, the static power consumption due to the leakage current can not be reduced and hence still remains.

[0004]   Since the operation speed of the CMOS circuit is decreased along with reduction of the power source voltage, in order to prevent the degradation of the operation speed, the threshold voltage of the MOS transistor needs to be reduced in conjunction with the reduction of the power supply voltage. However, since if the threshold voltage is reduced, then the leakage current is remarkably increased, along with the reduction of the power source voltage, the increase of the static power consumption due to the leakage current which was not conventionally large so much becomes remarkable. For this reason, it becomes a problem to realize a microprocessor in which the high speed is compatible with the low power consumption.

[0005]   As for a method of solving the problem associated with both the operation speed and the leakage current of the MOS transistor circuit, a method wherein the threshold voltage of the MOS transistor is controlled by setting variably the substrate biases is disclosed in JP-A-6-53496.

[0006]   The description will hereinbelow be given with respect to the device structure for use in setting variably the substrate biases with reference to Fig. 2. Fig. 2 shows a cross sectional view of a circuit having the CMOS structure. As shown in the figure, an n type well 205 is formed in a part of a surface layer of a p type well (p type substrate) 201, an n-channel MOS transistor consisting of an n^+ type source/drain region 202, a gate oxide film 203 and a gate electrode 204 is formed on a surface of the p type well 201, and a p-channel MOS transistor consisting of a p^+ type source/drain region 206, a gate oxide film 207 and a gate electrode 208 is formed on a surface of the n type well 205.

[0007]   Normally, the source of the p-channel MOS transistor and the source of the n-channel MOS transistor are respectively connected to the power source voltage (hereinafter, referred as Vdd) and the ground electric potential (hereinafter, referred as Vss), and the drains of the n-channel MOS transistor and the p-channel MOS transistor are connected to the output signal. As for terminals through which the substrate biases are given, Vbp 209 is provided in the n type well 205 of the p-channel MOS transistor, and Vbn 210 is provided in the p type well 201 of the n-channel MOS transistor.

[0008]   While when employing the device as shown in Fig. 2, normally, Vbp 209 is connected to Vdd and Vbn 210 is connected to Vss, during the non-operation of the circuits, these substrate biases are switched so that Vbp 209 is connected to the higher electric potential and Vbn 210 is connected to the lower electric potential, whereby the threshold voltages of the MOS transistors can be increased and hence the leakage current can be reduced.

DISCLOSURE OF THE INVENTION

[0009]   In order to realize a microprocessor in which the high speed operation is compatible with the low power consumption, it is required that for the processor circuitry, the variable control of the substrate biases as described above is carried out, and during the operation of the processor, the threshold voltages of the MOS transistors are decreased to maintain the high speed operation, while during the stand-by thereof, the threshold voltages are increased to reduce the leakage current. However, in order to control variably the substrate biases of the processor, the timing of reactivating the processor in the proceeding of the operation mode of the processor when switching the substrate biases, in particular in the proceeding of the operation mode from the stand-by state to the operation state is accurately controlled, whereby the malfunction of the processor must be prevented.

[0010]   The present invention was made in order to solve the above-mentioned problems, and it is therefore an object of the present invention to provide a high speed and low power consumption processor by realizing the above-mentioned substrate bias control, on a processor chip, which is applied to the various operation modes of the processor.

[0011]   In order to solve the above-mentioned prob-

lems, a feature of the present invention is provided by providing: a processor main circuit for executing program instruction strings on a processor chip; a substrate bias switching unit for switching voltages of substrate biases applied to a substrate of the processor main circuit; and an operation mode control unit for controlling, in response to the execution of an instruction to proceed to a stand-by mode in the processor main circuit, the substrate bias switching unit in such a way that the biases are switched over to voltages for the stand-by mode, and for controlling, in response to an interruption of the stand-by release from the outside, the substrate bias switching unit in such a way that the biases are switched over to voltages for a normal mode, and also for releasing, after the bias voltages switched thereto have been stabilized, the stand-by of the processor main circuit to restart the operation.

[0012]   In addition, another feature of the processor according to the present invention is that a semiconductor device of the processor chip has a triple well structure, and also the processor main circuit is formed on a well region different from those of the substrate bias switching unit and the operation mode control unit.

[0013]   In addition, still another feature of the processor according to the present invention is that the operation mode control unit includes, as means for waiting, before restarting the operation of the processor main circuit when switching the biases, until the bias voltages switched thereto are stabilized, either an on-chip timer for measuring a lapse of the time period required for stabilizing the biases, or a sensor for detecting that the biases have been stabilized to predetermined voltages.

[0014]   In addition, yet another feature of the processor according to the present invention is provided by providing: the processor main circuit in which the semiconductor device of the processor chip has a triple well structure and is divided into a plurality of functional modules which are respectively formed on the different wells; a substrate bias switching unit for switching the substrate biases to the substrate of the respective functional modules; a operation mode control unit for controlling, in response to execution to make stand-by one functional module or the plurality of functional modules in the processor main circuit, the substrate bias switching unit in such a way that the substrate biases of the one functional module or the plurality of functional modules are switched over to the voltages for the stand-by mode, and for controlling, when having received a signal to release the stand-by mode of the one functional module or the plurality of functional modules from the outside or the processor main circuit, the substrate bias switching unit in such a way that the biases are switched over to the voltages for a normal mode, and also for informing, after the bias voltages switched thereto have been stabilized, the processor main circuit of that the stand-by of the one functional module or the plurality of functional modules has been released.

[0015]   In addition, a further feature of the processor according to the present invention is provided by providing: means for switching dynamically the operation speed of the processor main circuit; and an operation mode control unit for controlling, in response to execution of an instruction to change the operation frequency in the processor main circuit, the substrate bias switching unit in such a way that the substrate biases of the processor main circuit or the functional modules are switched to voltages which are suitable for the operation frequency thereof, and for informing, after the bias voltages switched thereto have been stabilized, the processor main circuit of that the switching of the operation speed has been completed.

[0016]   Further, an even further feature of the processor according to the present invention is that the substrate bias switching unit is constituted by a substrate bias generating circuit for generating therein the voltages of the substrate biases.

[0017]   In addition, the present invention also proposes a control method contributing to the promotion of the low power consumption of the device. That is, since while the transistor having the low threshold is operated at a high speed, the leakage current passing between the source and the drain is large to increase the power consumption, it is important to prevent the large leakage current there-between.

[0018]   As for the construction therefor, there is provided a control method of controlling the power consumption of a semiconductor integrated circuit device including a plurality of element circuit blocks having transistors formed on a semiconductor substrate and being operated on the basis of a clock signal, wherein a first mode in which all the element circuit blocks are operated on the basis of the clock signal, a second mode in which the supply of the clock signal to at least one of the element circuit blocks is stopped, and a third mode in which the supply of the clock signal to all the element circuit blocks is stopped and also substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled to increase thresholds of the associated transistors are switched to be used.

[0019]   A main circuit is, for example, a processor including a CPU and the like. The first mode is a mode wherein the main circuit carries out the normal operation (computing, storage or the like).

[0020]   The second mode is a state in which the supply of the clock to a part of the processor is stopped, and is called a sleep mode, a deep sleep mode or the like for example. By selecting the range in which the clock is stopped, it is possible to promote the low power consumption while maintaining only the necessary functions.

[0021]   The third mode is a mode wherein the substrate biases are controlled for the circuits of the processor so as to increase the thresholds of the transistors constituting the circuits to reduce the power consumption due to the sub-threshold leakage current, and is

referred to as a stand-by mode or a hardware stand-by mode for example. While the operation mode can be returned from the stand-by mode to the normal state by the interruption control, in the hardware stand-by mode, the operation mode can be returned thereto by only the reset. In the third mode, the functions of the main circuit are stopped.

[0022] As for the construction of the overall circuitry, the element circuit blocks are included in a first circuit block, and the clock signal is formed from an oscillation circuit included in a second circuit block, and the clock signal and the information signals which are to be processed in the first circuit block are inputted from the second circuit block to the first circuit block. In addition to the oscillation circuit, an I/O circuit, and a control circuit for controlling the substrate biases are included in the second circuit block. Normally, the high speed operation is not required for the second circuit block so much as for the first circuit block. Then, it is desirable that the thresholds of the transistors constituting the second circuit block are larger than those of the transistors constituting the first circuit block and also the operation voltages of the former are higher than those of the latter. In addition, the transistors constituting the main circuit of the first circuit block are formed on the well different from those of other circuits, whereby the influence of other circuits thereupon can be reduced.

[0023] When the operation voltages of the first circuit block are different from those of the second circuit block, level conversion circuits are required to be provided between the first and second circuit blocks. For example, in order to carry out the conversion of the signal level, a level-down circuit is provided in the first circuit block, while a level-up circuit is provided in the second circuit block.

[0024] Since in the present invention, by switching the mode of the interest over to another mode, the substrate bias voltages are dynamically switched, in order to ensure the reliability, the operation sequence thereof is important.

[0025] When switching the operation mode from the first or second mode to the third mode, firstly, the clock signal which is inputted from the second circuit block to the first circuit block, and the information signals which are inputted to the first circuit block in order to be processed therein are stopped, and next, the substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled to increase the thresholds of the associated transistors. As a result, the input to the first circuit block in the state in which the operation of the first circuit block is unstable can be blocked and also the malfunction of the first circuit block can be prevented.

[0026] For this operation, the procedure may be adopted in which after the signal inputs to the first circuit block are stopped and the device waits for a predetermined time period (e.g., 60 μ sec. or so) through a timer or the like, the substrate biases are controlled. The timer for waiting is provided in the outside of the first circuit block, e.g., either in the second circuit block or in the outside of the device.

[0027] In addition, when switching the operation mode from the third mode (stand-by mode) to the first mode, the substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled to decrease the thresholds of the associated transistors, and next, the input of the above-mentioned clock signal which is inputted from the second circuit block to the first circuit block and the information signals which are to be processed in the first circuit block is started. That is, in order to prevent the malfunction of the first circuit block, after the substrate voltages of the first circuit block have been stabilized, the input of the signals is started.

[0028] For this reason, when switching the operation mode from the third mode to the first mode, after the substrate biases of the first circuit block are controlled to decrease the thresholds of the associated transistors and the device waits for a predetermined time period by the timer so that the operation is stabilized, the input of the clock signal which is to be inputted to the first circuit block and other signals is started.

[0029] Another method is such that after the state of the thresholds of the transistors have been confirmed by a voltage monitor or the like, the signal input to the first circuit block is started. Or, on the basis of the state of a substrate bias generating circuit for controlling the substrate voltages, in accordance with the signal which is outputted from the substrate bias generating circuit in order to report the stand-by release, the input of the clock signal and other signals which are to be inputted to the first circuit block is started.

[0030] As for a method of stopping the information signals and the clock signal to the first circuit block, it is considered that the signal levels are fixed by an output fixing circuit (level holding circuit) provided in the second circuit block. In the first mode, while the signals are inputted to the level-down circuit through the output fixing circuit, in the third mode, the inputs to the level-down circuit are fixed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031]

Fig. 1 is a block diagram of a processor chip in a first embodiment of the present invention;
Fig. 2 is a cross sectional view showing a general device structure for use in substrate bias control;
Fig. 3 is a cross sectional view showing a device structure in the first embodiment of the present invention;
Fig. 4 is a flow chart useful in explaining the operation in the first embodiment of the present invention;
Fig. 5 is a block diagram of a processor chip in a second embodiment of the present invention;

Fig. 6 is a block diagram of a processor chip in a third embodiment of the present invention;

Fig. 7 is a block diagram of a processor chip in a fourth embodiment of the present invention;

Fig. 8 is a block diagram of a processor chip in a fifth embodiment of the present invention;

Fig. 9 is a view useful in explaining the relation between the operation modes and the substrate bias control of the present invention;

Fig. 10 is a view useful in explaining a configuration of a processor main circuit of the present invention;

Fig. 11 is a view useful in explaining low power consumption modes of the present invention;

Fig. 12 is a view useful in explaining a sleep mode and a deep sleep mode of the present invention;

Fig. 13 is a transition diagram of the operation modes of the present invention;

Fig. 14 is a first structural view showing a configuration of the processor chip and a power source control circuit of the present invention;

Fig. 15 is a view useful in explaining a sequence of exchanging a power source of the present invention;

Fig. 16 is a second structural view showing a configuration of the processor chip and the power source control circuit of the present invention;

Fig. 17 is a view useful in explaining a sequence of RTC power source back-up of the present invention;

Fig. 18 is a view useful in explaining a sequence until return by interruption from the low power consumption mode of the present invention; and

Fig. 19 is a view useful in explaining a sequence until return by reset from the low power consumption mode of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0032]   Embodiments of the present invention will hereinafter be described with reference to the accompanying drawings.

[0033]   Fig. 1 is a block diagram showing an example of a configuration of a processor chip for realizing a first embodiment of the present invention. In Fig. 1, a processor chip 101 is an LSI having a circuit of a CMOS structure, and includes a processor main circuit 102, an operation mode control unit 103, and a substrate bias switching unit 104. To the substrate bias switching unit 104, voltages Vdd and Vss in the normal mode, and voltages Vddb and Vssb in the stand-by mode are inputted through a signal 110. In accordance with a signal 107 outputted by the operation mode control unit, the substrate bias switching unit 104 selects, as the substrate bias for a p-channel MOS transistor constituting the processor main circuit 102, between Vdd and Vddb to output the selected one to a signal Vbp 111, and also selects, as the substrate bias for an n-channel MOS transistor, between Vss and Vssb to output the selected

one to a signal Vbn 112. As for the voltage values for the substrate bias selection, for example, Vdd = 1.5V, Vddb = 3.0V, Vss = 0.0V and Vssb = -1.5V.

[0034]   Incidentally, as will be described later, a well 302 on which the processor main circuit 102 is formed is formed separately, independently of wells on which the substrate bias switching unit 104 and the operation mode control unit are respectively formed.

[0035]   Fig. 3 is a cross sectional view showing a device structure of the processor chip 101. A point of difference of Fig. 3 from Fig. 2 is that a p type well 302 is formed in an n type substrate 301 and the n type well 205 is formed in a part of the surface layer of the p type well 302, i.e., the device has a triple well structure. An n-channel MOS transistor is formed on the surface of the p type well 302 and a p-channel MOS transistor is formed on the surface of the n type well 205, thereby to constitute a CMOS circuit. In addition, a point that as for terminals through which the substrate biases are given, Vbp 209 is provided in the n type well 205 of the p-channel MOS transistor and Vbn 210 is provided in the p type well 302 of the n-channel MOS transistor is the same as in Fig. 2. In the present embodiment, the processor main circuit 102 is formed in the p type well 302 different from those of the operation mode control unit 103 and the substrate bias switching unit 104. As a result, the substrate bias control influences only the processor main circuit 102, and hence both the operation mode control unit 103 and the substrate bias switching unit 104 can avoid that influence.

[0036]   The description will hereinbelow be given with respect to the operation of the processor chip 101 in the present embodiment with reference to Fig. 4. The operation modes of the processor main circuit 102 are classified into the normal mode in which the normal instruction execution is carried out, and the stand-by mode in which the instruction execution is not carried out. Fig. 4 is a flow chart showing the processing on the processor chip 101 in the case where the operation mode of the processor main circuit 102 is changed from the normal mode to the stand-by mode and then is changed from the stand-by mode to the normal mode.

[0037]   Firstly, the processor main circuit 102 is operated in the normal mode. At this time, the sub-strate bias switching unit 104 selects Vdd and Vss for the substrate biases Vbp 111 and Vbn 112, respectively. For the voltage values of the substrate biases in the normal mode in this example, Vbp = 1.5V and Vbn = 0V (Step 401).

[0038]   After the processor main circuit 102 outputs, after having executed the sleep instruction, "stand-by request" to the signal 105 and then informs the operation mode control unit 103 of this fact, the processor main circuit 102 stops the operation of executing the instruction and then proceeds to the stand-by mode (Step 402).

[0039]   After having received the signal 105 from the processor main circuit, the operation mode control unit

103 outputs the signal 107 in order for the substrate biases of the processor main circuit 102 to be switched over to the voltages for the stand-by mode. Then, in response to the signal 107, the substrate bias switching unit 104 selects Vddb and Vssb, out of the input voltages 110, for the substrate biases Vbp 111 and Vbn 112, respectively, to output Vddb and Vssb (Steps 403 and 404). In this example, for the voltage values of the substrate biases in the stand-by mode, Vbp = 3.0V and Vbn = -1.5V.

[0040] When the operation mode control unit 103 detects that when the processor main circuit 102 is in the stand-by state, "stand-by release interruption" is asserted from the outside to a signal 108 (Step 405), the unit 103 outputs the signal 107 in order for the substrate biases of the processor main circuit 102 to be switched over to the voltages for the normal mode. Then, in response to the signal 107, the substrate bias switching unit 104 switches the substrate biases Vbp 111 and Vbn 112 over to Vdd (1.5V) and Vss (0.0V), respectively (Step 406).

[0041] Since there is the possibility that a lapse of some time period is required until the biases are stabilized after having switched the substrate biases, if the operation of the processor main circuit 102 is immediately restarted, then the malfunction may occur. In order to avoid this possibility, before switching the operation mode of the processor main circuit 102, the operation mode control unit 103 sets a sufficient time period required for stabilization of the substrate bias voltages switched thereto in an on-chip timer 109 and then restarts the processor main circuit 102 (Step 407) and then waits until time-out (Step 408). Then, after time-out, the operation mode control unit 103 outputs "stand-by release" to the signal 106 and then informs the processor main circuit 102 of this fact. In response to the signal 106, the processor main circuit 102 proceeds to the normal mode and restarts the operation of executing an instruction (Step 409).

[0042] In such a way as described above, the substrate biases Vbp 111 and Vbn 112 of the processor main circuit 102 are controlled such that during the operation, the threshold voltages of the MOS transistors constituting the processor main circuit are decreased to cope with the high speed operation, while during the stand-by, the threshold voltages thereof are increased to able to reduce the leakage current.

[0043] Fig. 5 is a block diagram showing a configuration of the processor chip in a second embodiment of the present invention. In the present embodiment, the operation mode control unit 103 includes a sensor 501 for detecting the bias voltages which are applied to the substrate of the processor main circuit 102. When the operation mode of the processor main circuit 102 is changed from the normal mode to the stand-by mode, the processing procedure in the above-mentioned first embodiment is applied to the present embodiment. On the other hand, when the operation mode of the proces-

sor main circuit 102 is changed from the stand-by mode to the normal mode, similarly to the above-mentioned embodiment, after the operation mode control unit 103 has controlled the substrate bias switching unit 104 so as to switch the substrate biases to the voltages for the normal mode, the unit 103 waits until the sensor 501 outputs the signal relating to the fact that the voltages of the substrate biases switched thereto are stabilized to the predetermined values, i.e., Vbp = 1.5V and Vbn = 0.0V in the present embodiment to a signal 502. When the sensor 501 outputs the stabilization of the substrate biases to the signal 502, then the operation mode control unit 103 outputs "stand-by release" to the signal 106 in order to restart the operation of the processor main circuit 102.

[0044] Fig. 6 is a block diagram showing a configuration of a processor chip in a third embodiment of the present invention. As for the basic device structure of a processor chip 601, the triple well structure as shown in Fig. 3 is assumed. In the processor chip 601 of Fig. 6, the processor main circuit includes a CPU 604, and a plurality of functional modules such as a module A 606 and a module B 608. The functional modules are present separately on the respective different well regions and hence one functional module is not influenced by the substrate bias control for other functional modules. The functional module includes the elements, each having the smaller scale unit, such as a CPU, an FPU, a cache, or a computing element. Substrate bias switching units 605, 607 and 609 are respectively provided so as to correspond to the functional modules 604, 606 and 608, and can switch, similarly to the above-mentioned embodiments, the substrate biases of the corresponding functional modules. The execution of the instruction is carried out with the CPU, as one of the functional modules, as a center, and hence if any instruction to make stand-by any unnecessary functional module for execution is executed, then the operation mode control unit 602 is informed of that the functional module of interest is in the stand-by state.

[0045] Next, the description will hereinbelow be given with respect to the operation of the processor chip 601 in the present embodiment. Firstly, it is assumed that all the functional modules are operated in the normal mode. After having executed the instruction to make stand-by the module A, the CPU 604 outputs the stand-by request to a signal 610, and thereafter, it is impossible to use that module until the stand-by of the module A 606 is released. After having received the signal 610, the operation mode control unit 602 outputs a signal 612 to the substrate bias switching unit 607 and then switches the substrate biases of the module A 606 over to the voltages for the stand-by mode. When the module A 606 is in the stand-by state, after the operation mode control unit 602 has received the signal 610 from the CPU 604 or a signal relating to the stand-by release of the module A 606 from the signal 613 outside of the processor chip 601, the unit 602 outputs the signal 612

to the substrate bias switching unit 607 and then switches the substrate biases of the module A over to the voltages for the normal mode. Then, similarly to the first embodiment of the present invention, the operation mode control unit 602 waits the stabilization of the substrate biases switched thereto using an on-chip timer 603, and after the stabilization thereof, informs the CPU 604 through a signal 611 of that the stand-by of the module A is released. After the CPU 604 has received this signal 611, it becomes possible to execute the instruction using the module A.

[0046]   The foregoing is applied to the stand-by control for the module B 608 as well as other functional modules. In addition, the CPU 604 itself is an object of the stand-by control. In this case, the functional module B 608 and other functional modules are controlled similarly to the case of the above-mentioned module A 604 except that after having proceeded to the stand-by mode, the CPU 604 stops all the instructions from being executed, and when the signal relating to the stand-by release of the CPU 604 has been asserted to the external signal 613, the operation mode control unit 602 asserts the stand-by release of the CPU 604 to the signal 611 after completion of the switching of the substrate biases of the CPU 604, thereby restarting the execution of the instructions of the CPU 604.

[0047]   By the stand-by control in functional modules in the present embodiment, it is possible to reduce the leakage current of any functional module which is unnecessary during the operation of the processor.

[0048]   Fig. 7 is a block diagram showing a configuration of a processor chip in a fourth embodiment of the present invention. A point of difference of the present embodiment from the first embodiment is that voltages 701 which are supplied from the outside to the substrate bias switching unit 104 are increased in kind so that the substrate bias switching unit 104 can select, as the substrate biases, the suitable voltages among these voltages 701 to apply them to the processor main circuit 102. In the present embodiment, it is assumed that means for changing dynamically the operation speed of the processor main circuit 102, i.e., the operation frequency thereof on the basis of an instruction, and the operation modes of the processor main circuit 102 are classified into a high speed mode and a low speed mode. In the present embodiment, Vdd (for the p-channel MOS transistor) and Vss (for the n-channel MOS transistor) are selected as the substrate biases corresponding to the high speed mode. Vddb2 (for the p-channel MOS transistor) and Vssb2 (for the n-channel MOS transistor) are selected as the substrate biases corresponding to the low speed mode, and Vddb1 (for the p-channel MOS transistor) and Vssb1 (for the n-channel MOS transistor) are selected as the substrate biases corresponding to the stand-by mode.

[0049]   Next, the description will hereinbelow be given with respect to the operation of the processor chip 101 in the present embodiment. Now, it is assumed that the operation mode of the processor main circuit 102 is switched from the high speed mode over to the low speed mode. While the processor main circuit 102 is being operated in the high speed mode, as the substrate biases for the processor main circuit, the substrate switching unit 104 selects Vdd and Vss for Vbp 111 and Vbn 112, respectively. After having executed the instruction to proceed to the low speed mode, the processor main circuit 102 outputs this request to the signal 105 to suspend the operation of executing the instruction. A clock which is supplied to the processor main circuit 102 is switched over to a low frequency on the basis of execution of the instruction to proceed to the low speed mode. After having received the signal 105, the operation mode control unit 103 outputs the signal 107 in order to switch the substrate biases of the processor main circuit 102 over to the voltages for the low speed mode. In response to the signal 107, the substrate bias switching unit 104 switches the substrate biases Vbp 111 and Vbn 112 over to Vddb2 and Vssb2, respectively. Similarly to the above-mentioned embodiments, the operation mode control unit 103 maintains the stability of the substrate biases switched thereto using the on-chip timer 109, and informs the processor main circuit 102 through the signal 106 of that the proceeding to the low speed mode has been completed. After having received the signal 106, the processor main circuit 102 restarts the suspended operation of executing the instruction in the low speed mode.

[0050]   Since the operation in switching the operation mode from the low speed mode to the high speed mode, in switching the operation mode from the high speed mode or the low speed mode to the stand-by mode, or in switching the operation mode from the stand-by mode to the high speed mode or the low speed mode in the present embodiment is also similar to the foregoing, the details thereof will be omitted here. In the present embodiment, it is also possible that the operation speed is further subdivided and the substrate bias control corresponding thereto is carried out. In addition, it is also possible as in the third embodiment, the processor main circuit 102 is separated in functional modules by utilizing the triple well structure of the device, and for every functional module, the substrate biases are controlled in conjunction with the switching of the operation frequency thereof.

[0051]   As in the present embodiment, the substrate bias control which is suitable for the operation frequency of the processor is carried out, whereby it is possible to reduce the leakage current in the low speed operation mode. In addition, since in the low speed mode, the range of the input voltages by which both the p-channel MOS transistor and the n-channel MOS transistor of the CMOS circuit are caused to conduct at the same time is narrower than that in the high speed operation mode, there is also provided the effect that the passing through current during the switching is reduced.

[0052]   Fig. 8 is a block diagram showing a configura-

tion of a processor chip in a fifth embodiment of the present invention. A point of difference of the present embodiment from the above-mentioned first embodiment is that the above-mentioned substrate bias switching unit is constituted by a substrate bias generating unit 801. The substrate bias generating circuit 801 is controlled by an output signal 802 of the operation mode control unit 103 so that it generates in the inside the voltages of the substrate biases to output these voltages to Vbp 111 and Vbn 112, respectively. The voltage values of the substrate biases Vbp 111 and Vbn 112 which are generated in correspondence to the operation mode of the processor main circuit 102 under the control by the operation mode control unit 103 are the same values as those in the first embodiment. Since the operations of the processor main circuit 102 and the operation mode control unit 103 are the same as those in the first embodiment, the details thereof will be omitted here. In addition, similarly to the present embodiment, the substrate bias switching unit in the second, third and fourth embodiments is constituted by the substrate bias generating circuit 801, whereby the substrate biases can be generated in the inside of the processor chip to switch the substrate biases thus generated in accordance with the operation mode.

[0053]   As described above, according to these embodiments, since the timing of reactivating the processor in the proceeding from the stand-by state to the operation state is accurately controlled using either the timer or the sensor, the optimal substrate bias control corresponding to the operation mode of the processor becomes possible. As a result, the leakage current can be reduced in the stand-by mode while maintaining the high speed when the operation mode of the processor is the normal mode. In addition, the substrate bias control is carried out in accordance with the operation mode by the functional module, whereby even when the processor is in operation, the leakage current of any functional module which is unnecessary for the execution can be reduced. Further, the substrate bias control which is suitable for the operation frequency of the processor is carried out, whereby in addition to the reduction of the leakage current in the low speed mode, there is also obtained the effect that the passing through current in the switching can be reduced.

[0054]   As a result, the reduction of the power consumption can be effectively realized and also it is possible to provide a microprocessor in which the high speed operation is compatible with the low power consumption.

[0055]   Hereinbelow, as an embodiment of a microcomputer, the operation mode in which the substrate biases are controlled will be described concretely. Then, it is assumed that the microcomputer has two power sources, i.e., a 1.8V power source and a 3.3V power source, and the substrate bias control is carried out by only the 1.8V power source. It is desirable that the circuit for supplying 1.8V is constituted by a MOS transis-

tor having a relative low threshold (e.g., Vth < 0.4V or so).

[0056]   Fig. 9 shows one example of the operation modes of the microcomputer. The operation modes are classified into a normal operation mode 981 in which the microcomputer is normally operated, and a reset mode 982. The modes in each of which the microcomputer is operated with the low power consumption are classified into a sleep mode 983, a deep sleep mode 984, a stand-by mode 985, a hardware stand-by mode 986, and an RTC (real time clock) battery back-up mode. In addition, as the test mode, there is an IDDQ measurement.

[0057]   Since the high speed operation is required during the normal operation 982, no control for the substrate biases is carried out. Since all the functions need to be reset during the reset 981, no control for the substrate biases is carried out. While in the low power consumption modes, no control for the substrate biases is carried out during the sleep 983 and the deep sleep 984 each having a short time period required for return from each of the low power consumption modes, in the case of the stand-by 985 and the hardware stand-by 986 in each of which emphasis is put on that the power consumption is reduced rather than the return time period, the substrate bias control is carried out. The RTC battery back-up mode is a mode wherein the voltage from only the power source for the RTC circuit operating at 3.3V is supplied. Since to the RTC battery back-up mode, the transition is made from the low power consumption mode, the substrate bias control is carried out. In addition, since the IDDQ measurement is a mode wherein the stand-by current is measured to measure the passing through current due to the short-circuit or the failure of the transistor, in this case, it is required that the substrate biases are necessarily controlled so as to reduce the leakage electric power of the chip to make the discovery of the failure easy.

[0058]   Prior to description of the low power consumption operation modes, the description will hereinbelow be given with respect to a configuration of internal blocks of a processor main circuit 902 with reference to Fig. 10. This figure is one example of the main constituent blocks of the processor main circuit. As for computing circuits, there are a CPU (central computing processing unit) 971 and an FPU (floating-point computing unit) 972. In addition thereto, there are a cache 973 as a memory self contained in the chip, a BSC (bus control unit) 974 for carrying out the interface with an external memory, a DMAC (DMA control unit) 975 for carrying out the DMA (direct memory access), an SCI (serial control unit) 976 for controlling a serial port, an INTC (interruption control unit) 977 for controlling an interruption input, a CPG (clock control unit) 978 for controlling a clock, and the like.

[0059]   The description will hereinbelow be given with respect to the sleep 983, the deep sleep 984 and the stand-by 985 as the low power consumption modes with

reference to Fig. 11.

[0060] In the sleep 983, only the clock for the computing units such as the CPU 971, the FPU 972, and the cache 973 is stopped and also the substrate bias control is not carried out. Therefore, though the power consumption can not be greatly reduced, the DMA transfer through the DMAC 975, and the normal refresh (refresh at the rate of 102 times/16 msec.) for the DRAM (dynamic RAM) and the SDRAM (synchronous dynamic RAM) through the BSC 974 are possible. Since the CPG 978 is in operation and the substrate bias control is not carried out, the time period required for return from the sleep 983 to the normal operation mode 982 is short.

[0061] Since in the stand-by 985 mode, all the operating clocks are stopped and also the substrate bias control is carried out, the power consumption is very small. Also, since all the clocks are stopped, it is impossible to carry out the DMA transfer. In addition, with respect to the refresh for the DRAM and the SDRAM, it is required that the control signals (RAS signal, CAS signal) for the memories are set using the BSC 974 in such a way that before entering into the stand-by 985, the mode becomes the self-refresh mode wherein the memories carry out the refresh by themselves. But, the time period required for return from the stand-by 985 to the normal operation 982 becomes long due to waiting for stability of the clock oscillation and a lapse of the time period required for return from the substrate biasing state since all the clocks are stopped.

[0062] The deep sleep 984 mode is the low power consumption mode between the sleep 983 and the stand-by 985.

[0063] The differences in operation modules between the sleep 983 and the deep sleep 984 are shown in Fig. 12. Since the BSC 973, the DMAC 974 and the SCI 975 which are operated during the sleep 983 are stopped during the deep sleep 984, the power consumption can be reduced so much.

[0064] But, in the deep sleep 984 mode, the DMA transfer can not be carried out and also the refresh of the memories becomes the self-refresh. The time period required for return from the deep sleep 984 to the normal operation 982 is, similarly to the sleep mode, short.

[0065] In such a way, the three kinds of low power consumption modes are provided, whereby the fine low power consumption control can be carried out in accordance with the application.

[0066] Fig. 13 shows a state transition diagram of the operation modes in order to give the description thereof. On the basis of a RESET# 952 (or, a power-on reset) pin input from a state 980 in which all the power sources are turned off, the processor chip makes transition to a reset state 981. When RESET# 952 is negated, the processor chip makes transition to the normal operation 982. Then, the processor chip makes transition from this state to the low power consumption operation mode.

[0067] There are two transition methods. One transition method is the transition based on an instruction. The CPU 971 executes a sleep instruction, thereby making this transition. A mode register is set in executing the sleep instruction, whereby the selection can be made among the sleep 983, the deep sleep 984 and the stand-by 985, and the processor chip can make transition to the selected one of these modes. The return from each of these modes to the normal operation mode 982 is carried out on the basis of an instruction 958.

[0068] The other transition method is the transition based on a HARDSTB# 951 pin. When having asserted this pin, the processor chip makes transition to a hardware stand-by state 986. This state is a state wherein similarly to the stand-by 985, all the clocks are stopped and also the substrate bias control is carried out too.

[0069] If in this mode, the impedance of an I/O buffer is made high, then no transistor having the passing through current flowing therethrough is present in the 3.3V system circuit, and hence the IDDQ measurement becomes possible.

[0070] In addition, if an input buffer of an RTC circuit provided in the 3.3V system circuit is fixed, even when the power sources for the constituent elements other than the RTC circuit are turned off, the input signal to the RTC circuit does not become at floating (at an intermediate level). Therefore, the malfunction of the RTC circuit can be prevented and only the RTC circuit can be operated.

[0071] Next, the description will hereinbelow be given with respect to an application example of the hardware stand-by.

[0072] Fig. 14 shows configurations of a processor chip 901 and a power source control circuit in which the hardware stand-by is applied to enable a power source (battery) 904 of the processor chip 901 to be exchanged.

[0073] The processor chip 901 is constituted by a 1.8V region circuit 930 which is operated at 1.8V and a 3.3V region circuit 931 which is operated at 3.3V. The 1.8V region circuit 930 includes a processor main circuit 902, and level-down circuits 905 and 906 each of which carries out the level conversion from 3.3V down to 1.8V. The 3.3V region circuit 931 includes a substrate bias generating circuit 903, a clock oscillation circuit 908, an I/O circuit 909, an operation mode control unit 913, an RTC circuit 914, level-up circuits 904 and 910 each of which carries out the level conversion from 1.8V up to 3.3V, and output fixing circuits 907 and 911 each of which fixes a signal from 3.3V to 1.8V.

[0074] A control circuit for a power source system includes a power source 904, a power source monitoring circuit 921, a display 921, and a voltage producing circuit 920 for producing a voltage for a 1.8V system.

[0075] The operation will hereinbelow be described. When the processor chip 901 is in the normal operation mode 982, the substrate bias generating circuit 903

holds the normal substrate levels (e.g., the electric potential VDD for the p-channel MOS transistor, and the electric potential VSS for the n-channel MOS transistor) without carrying out the subtraction with respect to the substrate biases. The clock generating circuit 908 includes a PLL (phase-locked loop) and the like, and produces a clock for the internal operation to send it to the processor main circuit 902 through the output fixing circuit 907 and the level-down circuit 905. The I/O circuit 909 fetches in a signal from the outside to send it to the processor main circuit 902 through the output fixing circuit 907 and the level-down circuit 905. In addition, the I/O circuit 909 outputs a signal from the processor main circuit 902 to the outside through the level-up circuit 904. The RTC circuit 914 is operated at 3.3V, and receives a control signal from the processor main circuit 902 through the level-up circuit 910 to transmit a control signal to the processor main circuit 902 through the level-down circuit 906 and the output fixing circuit 911. The operation mode control unit 913 carries out, in particular, the control for the substrate bias generating circuit 903.

[0076] The power source monitoring circuit 921 monitors the voltage level of the power source 904. When the voltage level has been decreased down to a level lower than a predetermined level (When having detected the exhaustion state of the battery), the circuit 921 makes HARDSTB# 951 the low level. At the same time, the circuit 921 displays the alarm for the battery exhaustion on the display 922 to inform a user of this fact. Even in the state in which the voltage level has been decreased, the voltage holding circuit 923 can hold the voltage level for a predetermined time period (ranging from several minutes to several hours). For this time period, a user can exchange the power source.

[0077] The description will hereinbelow be given with respect to a power source exchanging sequence with reference to Fig. 15.

(1) HARDSTB# 951 becomes the low level, whereby the operation mode enters into the hardware stand-by state 986. Now, 1.8V signal fixing 953 is outputted from the operation mode control unit 913 to fix the signal from 3.3V to 1.8V and also to stop a 1.8V system clock. As a result, even when carrying out the subtraction with respect to the substrate biases, the signal of 1.8V system is not operated. Therefore, the malfunction of the 1.8V system circuit in the state of carrying out the subtraction with respect to the substrate biases (the state in which since the threshold voltages of the MOS transistors are increases, the operation speed thereof is low and hence the substrate electric potentials are unstable) is prevented. In this state, a substrate bias control starting signal 955 is outputted to the substrate bias producing circuit 903.

(2) Thereafter, on the basis of the timing of the 1.8V signal fixing 953, the substrate bias control starting signal 955 is outputted to the substrate bias producing circuit 903. In actual, the signal is fixed between the signal fixing 953 and the substrate bias control start 955, and hence a time difference until the supply of the signals to the 1.8V region is stopped is set therein. This time difference can be measured by the timer bases on the RTC clock of the RTC circuit 914.

(3) In response to the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts carrying out the subtraction with respect to the substrate biases for the 1.8V system substrate. For a time period of carrying out the subtraction with respect to the substrate biases, a substrate bias in-control 956 signal is returned back to the operation mode control unit 913.

(4) In the state of carrying out the sub-traction with respect to the substrate biases, the processor main circuit 902 is not operated. In addition, since the leakage current is small, the consumption quantity of current is small. As a result, the hold time of the voltage holding circuit 923 becomes long.

(5) Under this state, the power source 904 is exchanged.

(6) Since after having exchanged the power source, the power source voltage recovers the normal level, HARDSTB# 951 returns to the high level.

(7) Thereafter, the power-on reset circuit is operated and RESET# 952 is inputted thereto. On the basis of this reset input, the substrate bias control starting signal 955 which is outputted from the operation mode control unit 913 is released.

(8) In response to release of the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts returning the substrate biases of the substrate to the electric potentials in the operation state (e.g., the electric potential VDD for the p-channel MOS transistor, and the electric potential VSS for the n-channel MOS transistor). A predetermined time period is required until recovery of the substrate biases, and after completion of the recovery of the substrate biases, the substrate bias in-control signal 956 is released to inform the operation mode control unit 913 of this result.

(9) In response to release of the substrate bias in-control signal 956, the 1.8V signal fixing 953 which is outputted from the operation mode control unit 913 is released, and then the signals are inputted to the 1.8V system circuits such as the processor main circuit 902 and the like.

(10) After completion of the reset state 981, the operation mode enters into the normal state 982, and the processor main circuit 902 starts the normal operation.

[0078] As described above, by utilizing the low power consumption mode by the hardware stand-by, the exchange of the power source 904 becomes possible.

[0079] Next, the description will hereinbelow be given with respect to a second application example of the hardware stand-by.

[0080] Fig. 16 shows an example of a configuration of realizing the RTC power source back-up mode. The RTC circuit 914 is called a real time counter and is provided for realizing the function such as a clock or a calendar. For this reason, the function of a clock can not be realized if the circuit 914 is not operated at all times. Even if the power source 904 is shut-off, the RTC circuit 914 needs to be operated.

[0081] In the embodiment shown here, in order to realize the RTC power source back-up mode, the 3.3V region is divided into a normal 3.3V region 991 and a region 992 in which the associated circuits are operated at 3.3V of the RTC. In addition, in the region of 3.3V of the RTC, both an input fixing circuit 912 and an input fixing level-up circuit 960 are added to the input circuit so that even when in the state in which other power sources (1.8V, the normal 3.3V power source) are shut-off, the input signal becomes at floating, the signal of an intermediate level is not transmitted to the region 992 in which the associated circuits are operated at 3.3V of the RTC. In such a way, the malfunction is prevented.

[0082] The control circuit for the power source system includes a back-up battery 962, and diodes 963 and 964 in addition to the power source 904, the power source monitoring circuit 921, the display 922, and the voltage producing circuit 920 for producing the voltage of 1.8V system.

[0083] The operation will hereinbelow be described. In the normal operation mode 982, the substrate bias generating circuit 903 holds the normal substrate levels without carrying out the subtraction with respect to the substrate biases. The clock oscillation circuit 908 includes a PLL (phased-locked loop) and the like, and produces a clock for the internal operation to send it to the processor main circuit 902 through both the output fixing circuit 907 and the level-down circuit 905. The I/O circuit 909 fetches in the signal from the outside and sends the signal thus fetched in to the processor main circuit 902 through both the output fixing circuit 907 and the level-down circuit 905. In addition, the circuit 909 outputs the signal from the processor main circuit 902 to the outside through the level-up circuit 904. The RTC circuit 914 is operated at 3.3V and receives the control signal from the processor main circuit 902 via the input fixing level-up circuit 960 to transmit the control signal to the processor main circuit 902 via both the level-down circuit 906 and the output fixing circuit 911. The operation mode control unit 913 receives the control signal via the input fixing circuit 912 to in particular carry out the control for the substrate bias generating circuit 903.

[0084] The voltage monitoring circuit 921 monitors the voltage level of the power source 904. When the voltage level has been decreased down to a level lower than a predetermined level (When having detected the state in which the battery is exhausted up), the circuit 921

makes HARDSTB# 951 a low level, and fixes the inputs to the RTC 3.3V region 992 to prevent the malfunction of the RTC circuit 914. At the same time, the circuit 921 displays the alarm of exhaustion of the battery on the display 922. Thereafter, the voltage level continues to be decreased so that the voltages of 3.3V and 1.8V systems will not be supplied to the processor chip 901. At this time, the voltages (VDD - RTC, VSS - RTC) are supplied to only the 3.3V region of the RTC from the back-up battery 962 via the diode 963, and hence even when the power source 904 is exhausted up, only the RTC circuit (the counter circuit for a calendar) 914 is normally operated. The diode 964 serves to prevent the current from being caused to flow through the circuits other than the RTC circuit 914.

[0085] The RTC power source back-up sequence will hereinbelow be described in detail with reference to Fig. 17.

(1) HARDSTB# 951 becomes a low level, whereby the operation mode enters into the hardware stand-by state 986. Then, the 1.8V signal fixing 953 is outputted from the operation mode control unit 913 to fix the signal from 3.3V to 1.8V and also to stop the clock of 1.8V system. As a result, since even when carrying out the subtraction with respect to the substrate biases, the signals of 1.8V system are not operated, the malfunction of the circuits of 1.8V system in the state of carrying out the subtraction with respect to the substrate biases is prevented. At the same time, the input fixing signal 954 to the RTC circuit 914 is outputted to fix the input signal. As a result, when other power sources are shut-off, the unstable signal of the intermediate level is prevented from entering into the RTC circuit 914.

(2) Thereafter, on the basis of the timing of the 1.8V signal fixing 953, the substrate bias control starting signal 955 is outputted to the substrate bias producing circuit 903. In actual, the signal is fixed between the signal fixing 953 and the substrate bias control state 955, and hence a time difference until the supply of the signals to the 1.8V region is stopped is set therein. This time difference can be measured by the timer based on the RTC clock of the RTC circuit 914.

(3) In response to the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts carrying out the subtraction with respect to the substrate biases of the substrate of 1.8V system. For a time period of carrying out the subtraction with respect to the substrate biases, the substrate bias in-control 956 signal is returned to the operation mode control unit 913.

(4) In the state of carrying out the subtraction with respect to the substrate biases, the processor main circuit 902 is not operated. In addition, since the leakage current is small, the consumption quantity of current is small.

(5) The shut-off time period of the power source 904 may be long. In addition, the power source 904 can be exchanged.

(6) Since after return from the shut-off of the power source 904 (or after exchange of the power source 904), the power source voltage recovers the normal level, HARDSTB# 951 is returned to the high level.

(7) Thereafter, the power-on reset circuit is operated and RESET# 952 is inputted. On the basis of this reset input, the substrate bias control starting signal 955 is released.

(8) In response to release of the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts returning the substrate biases of the substrate of 1.8V system to the electric potentials in the operation state (e,g., the electric potential VDD for the p-channel MOS transistor, and the electric potential VSS for the n-channel MOS transistor). A predetermined time period is required until recovery of the substrate biases, and after completion of the recovery of the substrate biases, on the basis of release of the substrate bias in-control signal 956, the operation mode control unit 913 is informed of the completion of the recovery.

(9) In response to release of the substrate bias in-control signal 956, the 1.8V signal fixing 953 which is outputted from the operation mode control unit 913 is released, and the signals are inputted to the circuits of 1.8V system such as the processor main circuit 902 and the like.

(10) After completion of the reset state 981, the operation mode enters into the normal state 982, and the processor main circuit 902 starts the normal operation.

[0086]   In the above-mentioned sequence, a power source switch is provided in the power source 904 so that for a time period when the power source is turned off, only the RTC circuit 914 can be operated.

[0087]   As described above, by utilizing the hardware stand-by, only the RTC circuit 914 can be operated on the basis of the back-up by the back-up battery.

[0088]   The description will hereinbelow be given with respect to the sequence in which by utilizing a normal sleep instruction 959, the operation mode enters into a stand-by state 985, and then on the basis of an interruption signal 958, the operation mode returns to the normal state 982 with reference to Fig. 18.

(1) On the basis of the sleep instruction 959, the operation mode enters into the stand-by state 985. Then, the 1.8V signal fixing 953 is outputted from the operation mode control unit 913 to fix the signal from 3.3V to 1.8V and also to stop the clock of 1.8V system. As a result, the malfunction of the circuits of 1.8V system when carrying out the subtraction with respect to the substrate biases is prevented.

(2) Thereafter, on the basis of the 1.8V signal fixing 953, the substrate bias control starting signal 955 is outputted to the substrate bias producing circuit 903. In actual, the signal is fixed between the signal fixing 953 and the substrate bias control state 955, and hence a time difference until the supply of the signals to the 1.8V region is stopped is set therein. This time difference can be measured by the timer based on the RTC clock of the RTC circuit 914.

(3) In response to the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts carrying out the subtraction with respect to the substrate biases of the substrate of 1.8V system. For a time period of carrying out the subtraction with respect to the substrate biases, the substrate bias in-control 956 signal is returned to the operation mode control unit 913.

(4) In the state of carrying out the subtraction with respect to the substrate biases, the processor main circuit 902 is not operated. In addition, since the leakage current is small, the consumption quantity of current is small.

(5) Under this state, after having received the interruption signal 958 from the control signal 957 (external pin) via the I/O circuit 909, the operation mode control unit 913 releases the substrate bias control starting signal 955.

(6) In response to release of the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts returning the substrate biases of the substrate of 1.8V system to the electric potentials in the operation state (e.g., the electric potential VDD for the p-channel MOS transistor, and the electric potential VSS for the n-channel MOS transistor). A predetermined time period is required until recovery of the substrate biases, and after completion of the recovery of the substrate biases, on the basis of release of the substrate bias in-control signal 956, the operation mode control unit 913 is informed of the completion of the recovery thereof.

(7) In response to release of the substrate bias in-control signal 956, the operation mode control unit 913 releases the 1.8V signal fixing 953. The 1.8V signal fixing 953 is released after having released the substrate bias in-control signal, whereby the malfunction of the circuits of 1.8V system is prevented.

(8) The signals are inputted to the circuits of 1.8V system such as the processor main circuit 902 and the like so that the operation mode enters into the normal state 982 and the processor main circuit 902 starts the normal operation.

[0089]   On the basis of the foregoing, the processor chip 901 enters into the low power consumption mode and also can return thereto by the interruption.

[0090]   The description will hereinbelow be given with

respect to the sequence in which by using the normal sleep instruction 959, the operation mode enters into the stand-by state 985 and then returns to the normal state 982 by RESET# 952 with reference to Fig. 19.

(1) On the basis of the sleep instruction 959, the operation mode enters into the stand-by state 985. Then, the 1.8V signal fixing 953 is outputted from the operation mode control unit 913 to fix the signal from 3.3V to 1.8V and also to stop the clock of 1.8V system. As a result, the malfunction of the circuits of 1.8V system when carrying out the subtraction with respect to the substrate biases is prevented.

Thereafter, it is measured that on the basis of the 1.8V signal fixing 953, the signal fixing has been completed, and then the substrate bias control starting signal 955 is outputted to the substrate bias producing circuit 903.

(2) In response to the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts carrying out the subtraction with respect to the substrate biases of the substrate of 1.8V system. For a time period of carrying out the subtraction with respect to the substrate biases, the substrate bias in-control 956 signal is returned to the operation mode control unit 913.

(3) In the state of carrying out the subtraction with respect to the substrate biases, the processor main circuit 902 is not operated. In addition, since the leakage current is small, the consumption quantity of current is small.

(4) Under this state, the operation mode control unit 913 receives RESET# 952 to release the substrate bias control starting signal 955.

(5) In response to release of the substrate bias control starting signal 955, the substrate bias generating circuit 903 starts returning the substrate biases of the substrate of 1.8V system to the electric potentials in the operation state. After completion of the return of the substrate biases, the operation mode control unit 913 is informed of the completion of the return using the substrate bias in-control signal 956.

(6) In response to this release signal, the 1.8V signal fixing 953 is released.

(7) After completion of the reset state 981, the signals are inputted to the circuits of 1.8V system such as the processor main circuit 902 and the like, and the operation mode enters into the normal state 982 and also the processor main circuit 902 starts the normal operation.

[0091] On the basis of the foregoing, the processor chip 901 enters into the low power consumption mode and also can return thereto by the reset.

[0092] As set forth hereinabove, the processor chip 901 has a section to which 1.8V is supplied as the power source voltage, and a section to which 3.3V is supplied as the power source voltage. The section to which 1.8V is supplied includes the processor main circuit 902 and the like for example. This section is a section wherein the circuit scale is large and the high speed operation is required. Since the circuit scale is large and also the high speed operation is required, the power consumption in this section becomes large. In the present embodiment, the power source voltage is reduced in order to reduce that power consumption.

[0093] In addition, since if the power source voltage is decreased (e.g., 1.8V), then the operation speed becomes slow, the threshold voltages of the MOS transistors are decreased (e.g., Vth < 0.4V or so). In addition, in the present embodiment, the substrate voltage control is carried out in order to reduce the sub-threshold leakage current due to the decrease of the threshold voltage.

[0094] On the other hand, the section to which 3.3V is supplied as the power source voltage includes the RTC circuit 914 and the like for example. Since these circuits are small in scale and are operated at the low speed, the power consumption is small. Therefore, for such circuit blocks, the power source voltage does not need to be decreased. For example, the relation of Vth > 0.5V or so can be established. Thus, since the threshold voltage of the MOS transistor does not need to be decreased, there is obtained the advantage that the current measure by the substrate control is not required in order to reduce the sub-threshold leakage current.

[0095] The processor chip 901 of the present embodiment uses both the power source voltages appropriately. That is, for the section requiring the large scale high speed operation, the MOS having the low threshold voltage is used by controlling the substrate, and also the MOS transistor having the high threshold voltage is used without controlling the substrate. While the method of manufacturing the MOS transistors having the different threshold values is not limited in particular, it can be realized by changing the channel implantation quantity. In addition, it can be realized by changing the thickness of the gate oxide film. In the latter, the technique may be adopted wherein for the construction of the MOS transistor, the oxide film is thickened to increase the threshold voltage. This reason is that since the MOS transistor having the high threshold voltage is operated at a high voltage, the oxide film b needs to be thickened. If the threshold voltage can be increased by thickening the oxide film, then the process can be simplified.

[0096] In addition, since the I/O circuit 909 needs to transmit/receive the external signal amplitude of 3.3V, if the MOS transistor which is the same as the MOS transistor having the high threshold voltage is employed therefor, then the process can be desirably made common thereto.

Claims

1. A microprocessor comprising:

   a main circuit including transistors;
   a substrate bias switching circuit for switching voltages of substrate biases applied to a substrate of said main circuit; and
   an operation mode control circuit for controlling, in response to execution of an instruction to proceed to a first mode in said main circuit, said substrate bias switching circuit in such a way that the substrate biases are switched over to voltages for the first mode, and for controlling, in response to execution of an instruction to proceed to a second mode in said main circuit, said substrate bias switching circuit in such a way that the substrate biases are switched over to voltages for the second mode, and also for starting, when switching the substrate biases from the voltages for the first mode over to the voltages for the second mode, the operation of said transistors of said main circuit after the bias voltages switched thereto have been stabilized.

2. A microprocessor according to claim 1, wherein the substrate in which said microprocessor is formed has a triple well structure in which a second semiconductor region of a second type is formed within a first semiconductor region of a first type, and a third semiconductor region of the first type is formed within said semiconductor region of the second type.

3. A microprocessor according to claim 2, wherein an n-channel transistor is formed on said second semiconductor region and also a p-channel transistor is formed on said third semiconductor region.

4. A microprocessor according to claim 2 or 3, wherein said substrate bias switching circuit controls a voltage applied to said second semiconductor region and a voltage applied to said third semiconductor region.

5. A microprocessor according to one of claims 1 to 4, wherein said main circuit is formed on a well region which is different from those of said substrate bias switching circuit and said operation mode control circuit.

6. A microprocessor according to one of claims 1 to 5, wherein said operation mode control circuit includes a timer for measuring a lapse of a time period required for stabilization of the biases.

7. A microprocessor according to one of claims 1 to 5,

wherein said operation mode control circuit includes a sensor for detecting that the biases have been stabilized to predetermined voltages, respectively.

8. A microprocessor according to one of claims 1 to 7, wherein said substrate bias switching circuit includes a substrate bias generating circuit for generating voltages for the substrate biases.

9. A microprocessor according to one of claims 1 to 8, wherein said first mode is a stand-by mode wherein the operation of said main circuit becomes stand-by, and also said second mode is a normal mode wherein said main circuit carries out a normal operation.

10. A microprocessor according to one of claims 1 to 9, wherein said first mode is a state in which the power consumption of said main circuit becomes smaller than that in said second mode.

11. A microprocessor according to one of claims 1 to 10, wherein said main circuit includes: a CPU, a cache memory for inputting/outputting data to/from said CPU, an interruption control circuit for controlling an interruption input, and a clock control circuit for controlling a clock.

12. A microprocessor according to claim 11, wherein in said first mode, the clock for said main circuit is stopped.

13. A microprocessor according to one of claims 1 to 12, further comprising a battery as the power source of said main circuit, and a monitoring circuit for monitoring a voltage of said battery, wherein when the voltage of said battery is reduced to a level lower than a predetermined value, said second mode is switched over to said first mode on the basis of a control signal from said monitoring circuit.

14. A microprocessor according to claim 12, wherein after having stopped the clock for said main circuit, the operation mode enters into said first mode.

15. A microprocessor comprising:

   a processor main circuit for executing program instruction strings;
   a substrate bias control circuit for controlling substrate biases applied to a substrate on which said processor main circuit is formed; and
   an operation mode control unit for controlling said substrate bias control circuit in such a way that said processor main circuit is controlled so

as to obtain voltages for a stand-by mode, and for controlling, in response to an interruption for the stand-by release from the outside, said substrate bias control circuit in such a way that the voltages for the stand-by mode are switched over to voltages for a normal mode, wherein said operation mode control unit releases the stand-by of said main circuit after the voltages for the normal mode have been stabilized.

16. A semiconductor integrated circuit device having a first circuit block including transistors and a second circuit block for exchanging signals between said first circuit block and said second circuit block, said device comprising:

a substrate bias generating circuit for applying substrate bias voltages to a semiconductor substrate on which the transistors of said first circuit block are formed; and
output fixing circuits for fixing, when said substrate bias generating circuit changes the substrate bias voltages, levels of at least part of the signals which are inputted from said second circuit block to said first circuit block.

17. A semiconductor integrated circuit device according to claim 16, wherein said first circuit block is different in operation voltages from said second circuit block.

18. A semiconductor integrated circuit device according to claim 16 or 17, further comprising an operation mode control unit for receiving, as an input, a substrate bias in-control signal from said substrate bias control circuit, wherein said output fixing circuits are controlled on the basis of a signal fixing signal from said operation mode control circuit.

19. A semiconductor integrated circuit device according to one of claims 16 to 18, wherein said substrate bias generating circuit is arranged in said second circuit block.

20. A semiconductor integrated circuit device according to one of claims 16 to 19, comprising said output fixing circuits for fixing levels of at least part of the signals which are inputted from said second circuit block to said first circuit block, when said substrate bias generating circuit changes the substrate bias voltages in such a way that thresholds of the transistors become high.

21. A semiconductor integrated circuit device having a first circuit block including transistors and a second circuit block for exchanging signals between said first circuit block and said second circuit block, said

device comprising:

a substrate bias generating circuit for applying substrate bias voltages to a semiconductor substrate on which the transistors of said first circuit block are formed; and
a clock oscillation circuit for stopping a clock signal inputted to said first circuit block, when said substrate bias generating circuit changes the substrate bias voltages.

22. A semiconductor integrated circuit device according to claim 21, wherein said first circuit block is different in operation voltages from said second circuit block.

23. A semiconductor integrated circuit device according to claim 21 or 22, further comprising an output fixing circuit for fixing a level of an output signal of said clock oscillation circuit.

24. A semiconductor integrated circuit device according to one of claims 21 to 23, wherein said clock oscillation circuit is arranged in said second circuit block.

25. A semiconductor integrated circuit device according to one of claims 21 to 24, comprising said clock oscillation circuit for stopping the signal inputted to said first circuit block, when said substrate bias generating circuit changes the substrate bias voltages in such a way that the thresholds of the transistors become high.

26. A semiconductor integrated circuit device comprising: a first circuit block including a logical circuit having MOS FETs, and driven by a first voltage; and a second circuit block including an I/O circuit, a level holding circuit and a bias generating circuit, and driven by a second voltage,
wherein said bias generating circuit switches voltages applied to said main circuit in such a way that thresholds of the MOS FETs become high;

an output signal from said I/O circuit is inputted to said main circuit through an output fixing circuit; and
when switching the voltages by said bias generating circuit, said output fixing circuit fixes the output signal.

27. A semiconductor integrated circuit device according to claim 26, wherein a clock oscillation circuit is provided in said second circuit block, and when switching the voltages by said bias generating circuit, said output fixing circuit fixes the clock signal.

28. A semiconductor integrated circuit device according to claim 26 or 27, wherein a clock oscillation circuit

is provided in said second circuit block, and a clock signal is supplied from said clock oscillation circuit to said main circuit, and when switching the voltages by said bias generating circuit and during the switching, the supply of the clock signal to said main circuit is stopped.

29. A semiconductor integrated circuit device according to one of claims 26 to 28, wherein said bias generating circuit switches the voltages supplied to said main circuit in such a way that thresholds of the MOS FETs of said main circuit become high, whereby said main circuit is switched from a normal operation mode over to a stand-by mode having the power consumption smaller than that of the normal operation mode.

30. A semiconductor integrated circuit device according to claim 29, wherein said main circuit includes a logical circuit, and in the greater part of the normal operation mode, said logical circuit functions.

31. A semiconductor integrated circuit device according to Claim 30, wherein when switching said main circuit from the stand-by mode over to the normal mode by switching by said bias generating circuit the voltages supplied to said main circuit in such a way that the thresholds of the MOS FETs of said main circuit become low, said logical circuit starts functioning at a time point later than the time point of switching the voltages.

32. A semiconductor integrated circuit device according to claim 31, wherein after the voltages supplied to said main circuit have been stabilized, the operation of the MOS FETs of said main circuit is started.

33. A semiconductor integrated circuit device according to one of claims 26 to 32, wherein a substrate on which the MOS FETs are formed has a triple well structure in which a second semiconductor region of a second type is formed within a first semiconductor region of a first type, and a third semiconductor region of the first type is formed within said semiconductor region of the second type.

34. A processor comprising: a processor main circuit for executing program instruction strings on a processor chip; a substrate bias switching unit for switching voltages of substrate biases applied to a substrate of said processor main circuit; and an operation mode control unit for controlling, in response to the execution of an instruction to proceed to a stand-by mode in said processor main circuit, said substrate bias switching unit in such a way that the biases are switched over to voltages for the stand-by mode, and for controlling, in response to an interruption of the stand-by release from the out-

side, said substrate bias switching unit in such a way that the biases are switched over to voltages for a normal mode, and also for releasing, after the bias voltages switched thereto have been stabilized, the stand-by of said processor main circuit to restart the operation.

35. A processor according to claim 34, wherein a semiconductor device of said processor chip has a triple well structure, and said processor main circuit is formed on a well region which is different from those of said substrate bias switching unit and said operation mode control unit.

36. A processor according to claim 34, wherein said operation mode control unit includes, as means for waiting, before restarting the operation of said processor main circuit when switching the biases, until the bias voltages switched thereto are stabilized, an on-chip timer for measuring a lapse of a time period required for stabilization of the biases.

37. A processor according to claim 34, wherein said operation mode control unit includes, as means for waiting, before restarting the operation of said processor main circuit when switching the biases, until the bias voltages switched thereto are stabilized, a sensor for detecting that the biases have been stabilized to predetermined voltages, respectively.

38. A processor according to claim 34, comprising: said processor main circuit in which a semiconductor device of said processor chip has a triple well structure and is divided into a plurality of functional modules which are formed on different well regions, respectively;

said substrate bias switching unit for switching the substrate biases applied to the substrate of said functional modules; and said operation mode control unit for controlling, in response to the execution of an instruction to make stand-by said one functional module or said plurality of functional modules in said processor main circuit, said substrate bias switching unit in such a way that the substrate biases of said one functional module or said plurality of functional modules are switched over to voltages for the stand-by mode, and for controlling, in response to a signal of the stand-by release of said one functional module or said plurality of functional modules from the outside or said processor main circuit, said substrate bias switching unit in such a way that the biases are switched over to voltages for a normal mode, and also for informing, after the bias voltages switched thereto have been stabilized, said processor main circuit of that the stand-by of

said one functional module or said plurality of functional modules has been released.

39. A processor according to claim 34 or 37, further comprising: means for switching dynamically the operation speed of said processor main circuit; and

said operation mode control unit for controlling, in response to the execution of an instruction to change the operation speed in said processor main circuit, said substrate bias switching unit in such a way that the substrate biases of said processor main circuit or said functional modules are switched over to voltages which are suitable for the operation frequency thereof, and for informing, after the bias voltages switched thereto have been stabilized, said processor main circuit of that the switching of the operation speed has been completed.

40. A processor according to claim 34 or 37, wherein said substrate bias switching unit is constituted by a substrate bias generating circuit for generating therein the voltages of the substrate biases.

41. A control method of controlling the power consumption of a semiconductor integrated circuit device including a plurality of element circuit blocks having transistors formed on a semiconductor substrate and operated on the basis of a clock signal, wherein a first mode in which all said element circuit blocks are operated on the basis of the clock signal, a second mode in which the supply of the clock signal to at least one of said element circuit blocks is stopped, and a third mode in which the supply of the clock signal to all said element circuit blocks is stopped and also substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled so as to increase thresholds of the associated transistors are switched to be used.

42. A method of controlling a semiconductor integrated circuit device according to claim 41, wherein said element circuit blocks are included in a first circuit block, and the clock signal is produced from an oscillation circuit included in a second circuit block, and also the clock signal and information signals which are to be processed in said first circuit block are inputted from said second circuit block to said first circuit block.

43. A method of controlling a semiconductor integrated circuit device according to claim 42, wherein when switching the operation mode to said third mode, the clock signal and the information signals which are to be processed in said first circuit block are stopped from being inputted from said second circuit block to said first circuit block, and next, the substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled so as to increase the thresholds of the associated transistors.

44. A method of controlling a semiconductor integrated circuit device according to claim 43, wherein when switching the operation mode to said third mode, after the clock signal and the information signals which are to be processed in said first circuit block have been stopped from being inputted from said second circuit block to said first circuit block, and said device waits for a lapse of a predetermined time period using a timer, the substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled so as to increase the thresholds of the associated transistors.

45. A method of controlling a semiconductor integrated circuit device according to claim 42, wherein when switching the operation mode from said third mode to said first mode, the substrate biases of at least part of the transistors formed on the semiconductor substrate are controlled so as to decrease the thresholds of the associated transistors, and next, the clock signal and the information signals which are to be processed in said first circuit block are started being inputted from said second circuit block to said first circuit block.

46. A method of controlling a semiconductor integrated circuit device according to claim 45, wherein when switching the operation mode from said third mode to said first mode, after the substrate biases of at least part of the transistors formed on the semiconductor substrate have been controlled so as to decrease the thresholds of the associated transistors, and said device waits for a lapse of a predetermined time period, the clock signal and the information signals which are to be processed in said first circuit block are started being inputted from said second circuit block to said first circuit block.
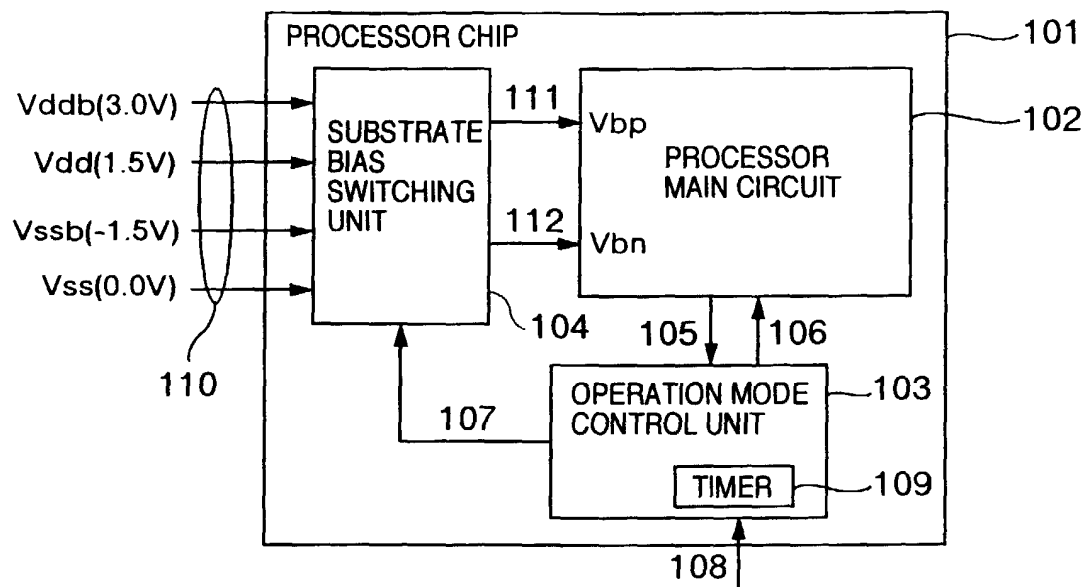
47. A method of controlling a semiconductor integrated circuit device according to claim 45, wherein when switching the operation mode from said third mode to said first mode, after the substrate biases of at least part of the transistors formed on the semiconductor substrate have been controlled so as to decrease the thresholds of the associated transistors, and the state of the thresholds of the associated transistors is confirmed, the clock signal and the information signals which are to be processed in said first circuit block are started being inputted from said second circuit block to said first circuit block.
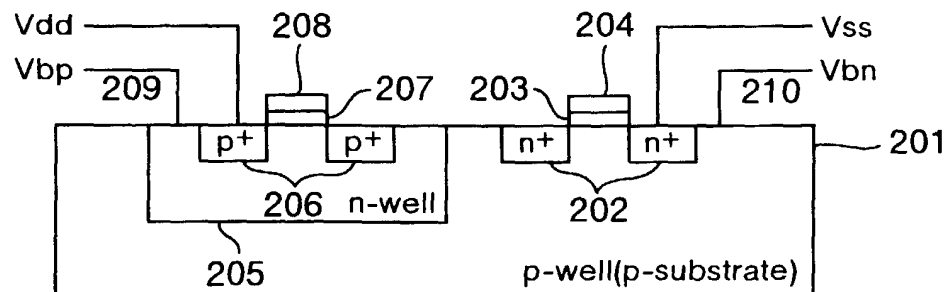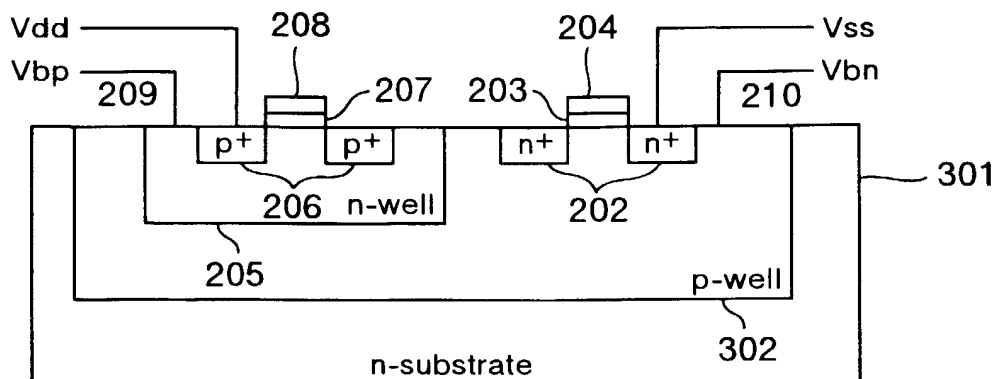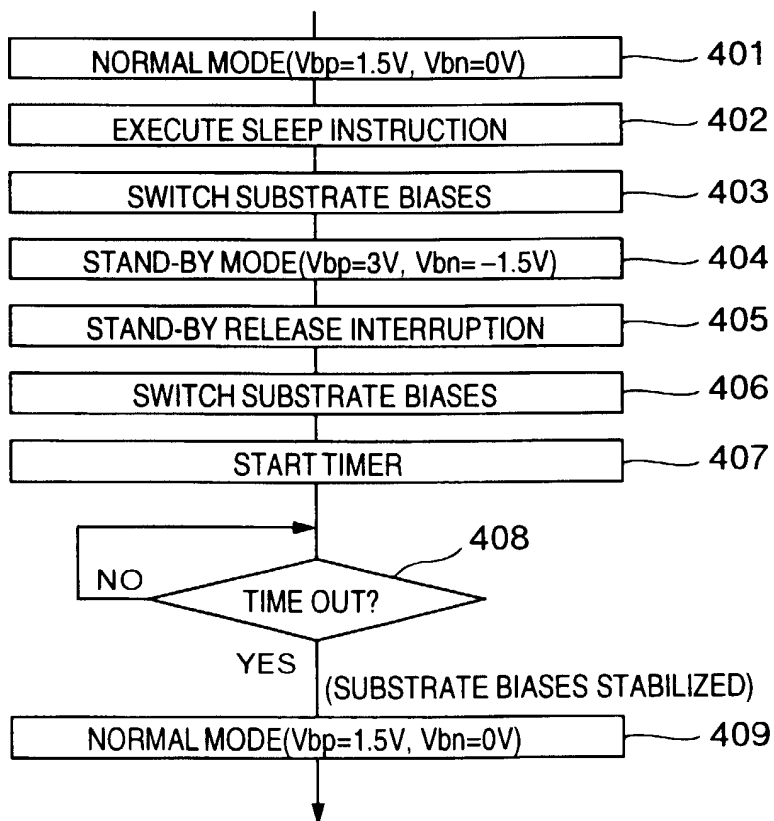
FIG.1

PROCESSOR CHIP — 101

Vddb(3.0V)
Vdd(1.5V)
Vssb(-1.5V)
Vss(0.0V)

110

SUBSTRATE
BIAS
SWITCHING
UNIT

104

111 → Vbp
112 → Vbn

PROCESSOR
MAIN CIRCUIT — 102

105 ↓ ↑ 106

107

OPERATION MODE
CONTROL UNIT — 103

TIMER — 109

108

FIG.2

Vdd
Vbp — 209

208
207
p+   p+
206   n-well
205

204
203
n+   n+
202
p-well(p-substrate)

Vss
210 — Vbn

201

FIG.3

Vdd —

Vbp — 209

208

207

204

203

210

Vss —

Vbn —

p+ p+

206 n-well

205

n+ n+

202

301

p-well

302

n-substrate

FIG.4

| NORMAL MODE(Vbp=1.5V, Vbn=0V) | 401 |

| EXECUTE SLEEP INSTRUCTION | 402 |

| SWITCH SUBSTRATE BIASES | 403 |

| STAND-BY MODE(Vbp=3V, Vbn= –1.5V) | 404 |

| STAND-BY RELEASE INTERRUPTION | 405 |

| SWITCH SUBSTRATE BIASES | 406 |

| START TIMER | 407 |

408

NO

TIME OUT?

YES (SUBSTRATE BIASES STABILIZED)

| NORMAL MODE(Vbp=1.5V, Vbn=0V) | 409 |

FIG.5

PROCESSOR CHIP — 101

Vddb(3.0V)
Vdd(1.5V)
Vssb(-1.5V)
Vss(0.0V)

110

SUBSTRATE BIAS SWITCHING UNIT

111 Vbp

112 Vbn

104

PROCESSOR MAIN CIRCUIT — 102

105 106 SENSOR

107

OPERATION MODE CONTROL UNIT

103

502 501

108

FIG.6

601

PROCESSOR CHIP

605 604 607 606 609 608

Vddb
Vdd

614

Vbp
CPU
Vbn

Vbp
Module A
Vbn

Vbp
Module B
Vbn

Vssb
Vss

612

611

610

OPERATION MODE CONTROL UNIT — 602

TIMER — 603

613

FIG.7

FIG.8

FIG.9

OPERATION MODE	SUBSTRATE BIAS CONTROL
RESET	NO CONTROL
NORMAL OPERATION	NO CONTROL
SLEEP	NO CONTROL
DEEP SLEEP	NO CONTROL
STAND-BY	CONTROL
HARD WARE STAND-BY	CONTROL
RTC BATTERY BACK-UP	CONTROL
IDDQ MEASUREMENT	CONTROL

981
982
983
984
985
986

FIG.10
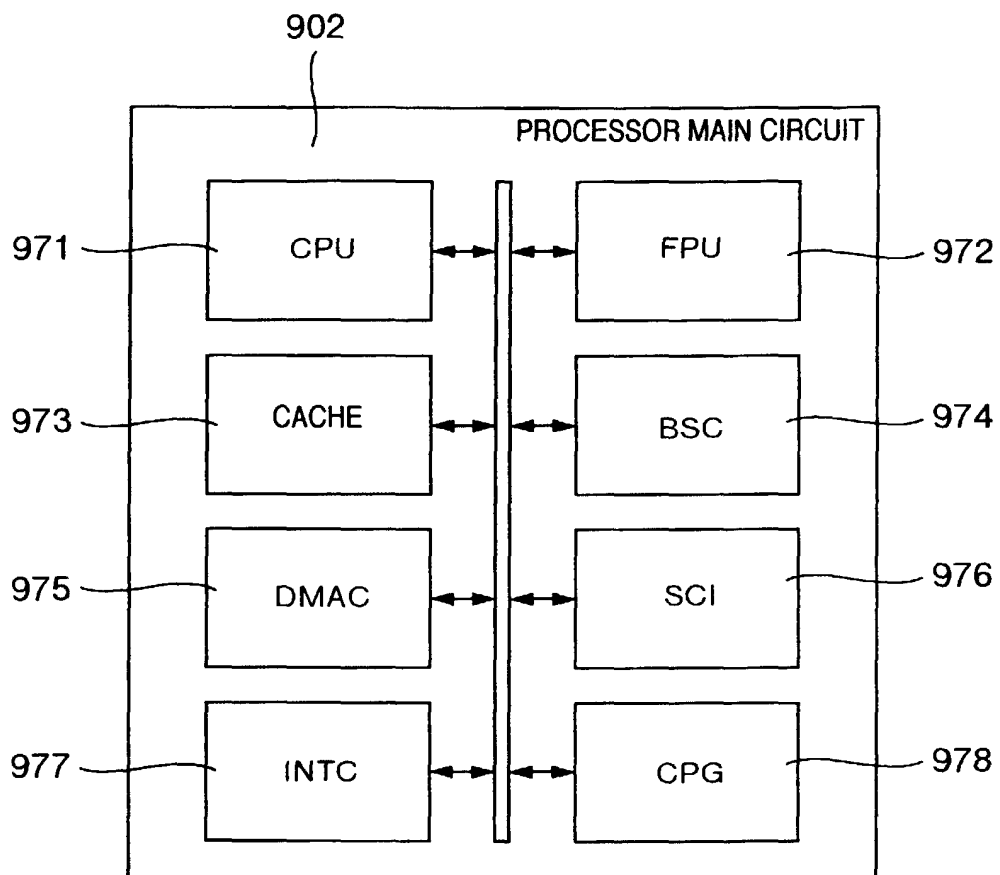
FIG.11

	SLEEP	DEEP SLEEP	STAND-BY
	983	984	985
POWER CONSUMPTION	△	○	◎
DMA TRANSFER	POSSIBLE	INHIBIT	INHIBIT
MEMORY REFRESH	NORMAL REFRESH	SELF-REFRESH	SELF-REFRESH
RETURN TIME	SHORT	SHORT	LONG
SUBSTRATE BIAS CONTROL	NO CONTROL	NO CONTROL	CONTROL

FIG.12

		SLEEP	DEEP SLEEP
971	CPU	STOP	STOP
972	FPU	STOP	STOP
973	CACHE	STOP	STOP
974	BSC	OPERATE	STOP
975	DMAC	OPERATE	STOP
976	SCI	OPERATE	STOP
977	INTC	OPERATE	OPERATE
978	CPG	OPERATE	OPERATE

983 984

FIG.13

FIG.14

FIG.15

FIG.16

901

FIG.17

950

POWER
SOURCE LEVEL

951 ─── HARDSTB#

952 ─── RESET#

982 | 986 | 981 | 982

953 ─── OPERATION MODE   NORMAL ╳ HARD WARE STAND-BY ╳ ╳ NORMAL

1.8V SIGNAL FIXING   RESET

954 ─── FIXING INPUT TO
RTC CIRCUIT

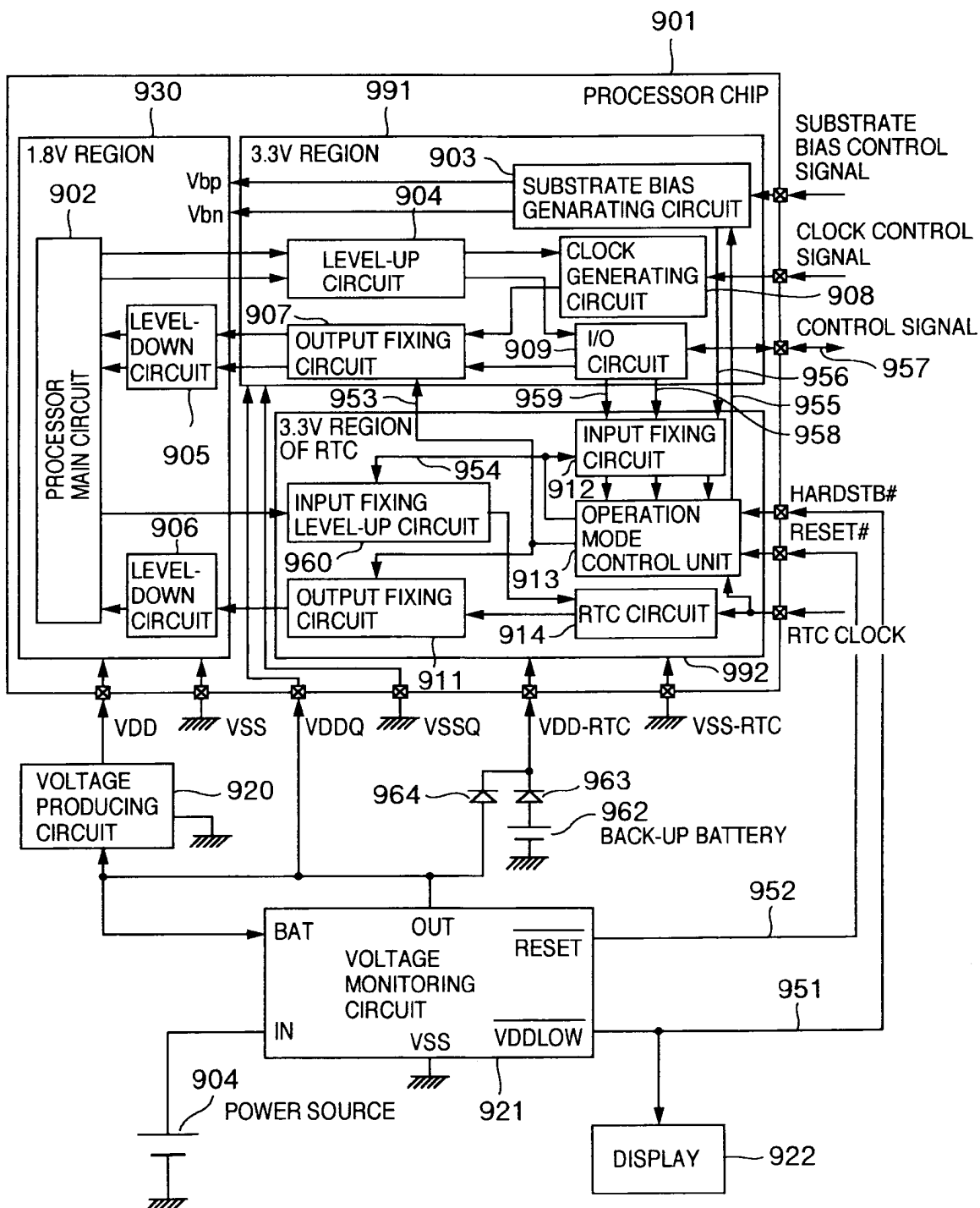955 ─── SUBSTRATE BIAS
CONTROL START

SUBSTRATE BIAS
IN-CONTROL

956
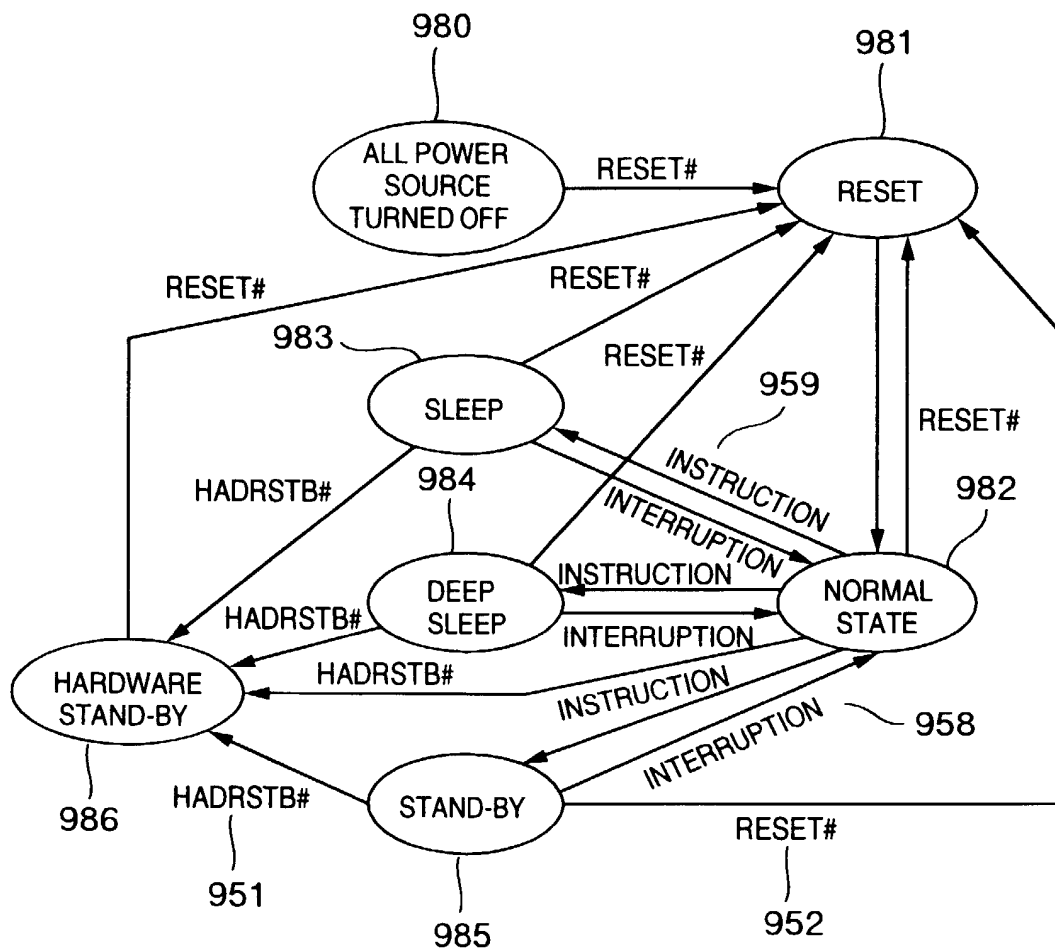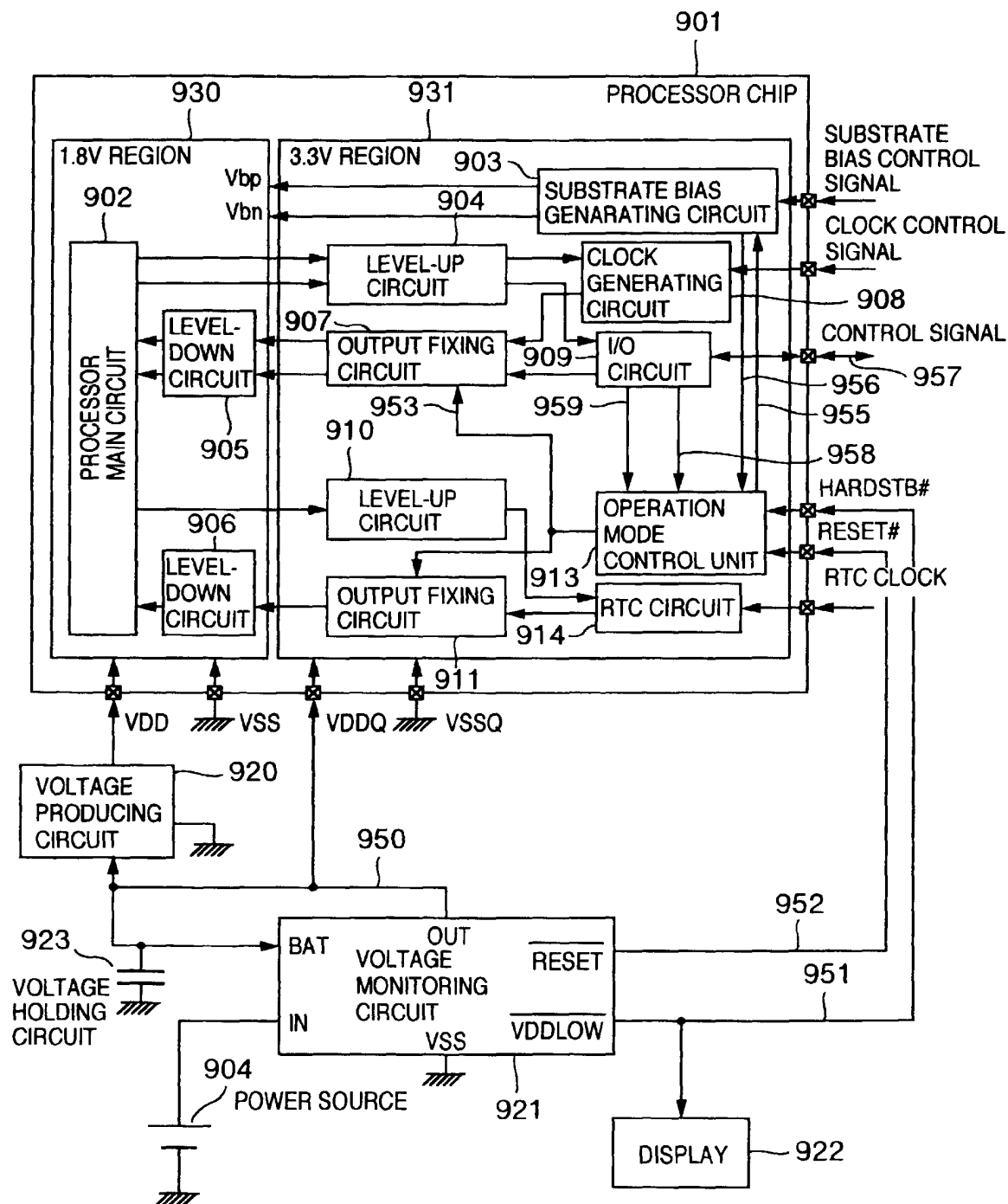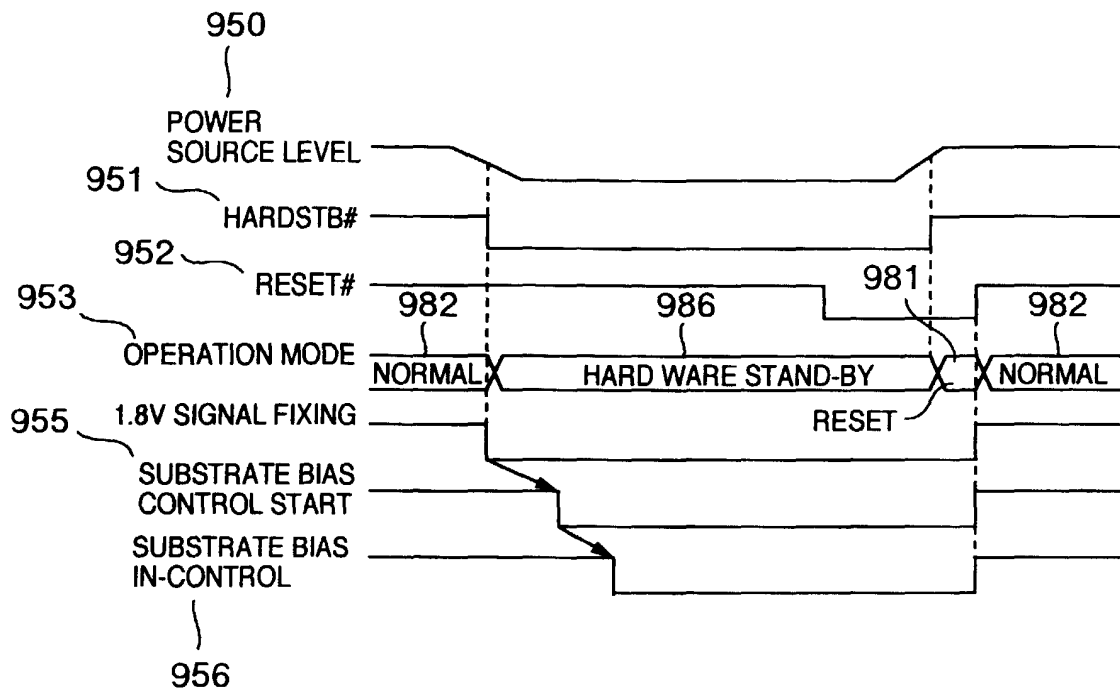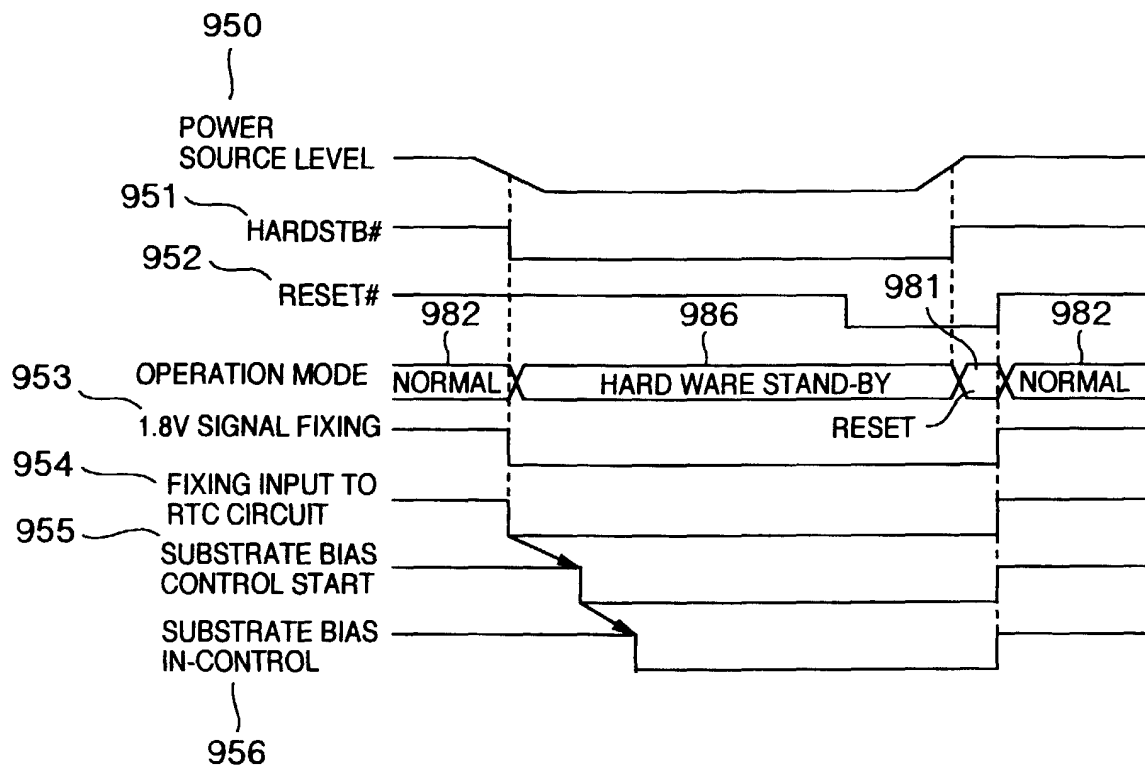
FIG.18
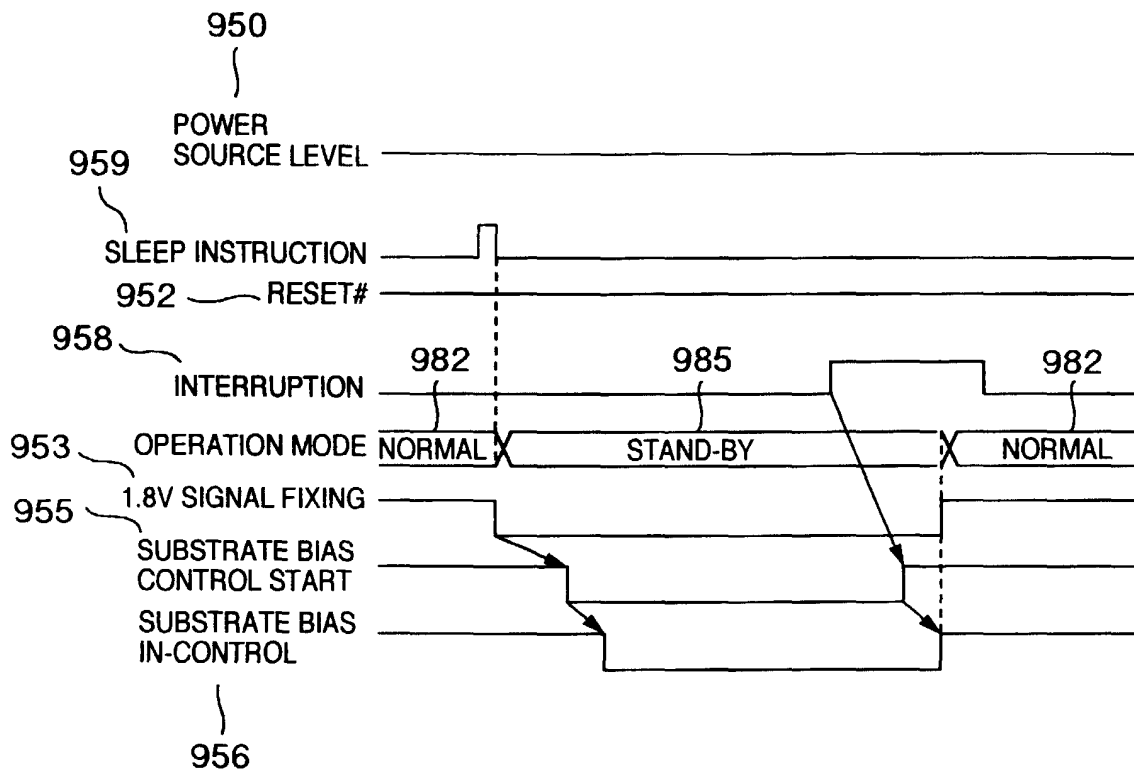
FIG.19
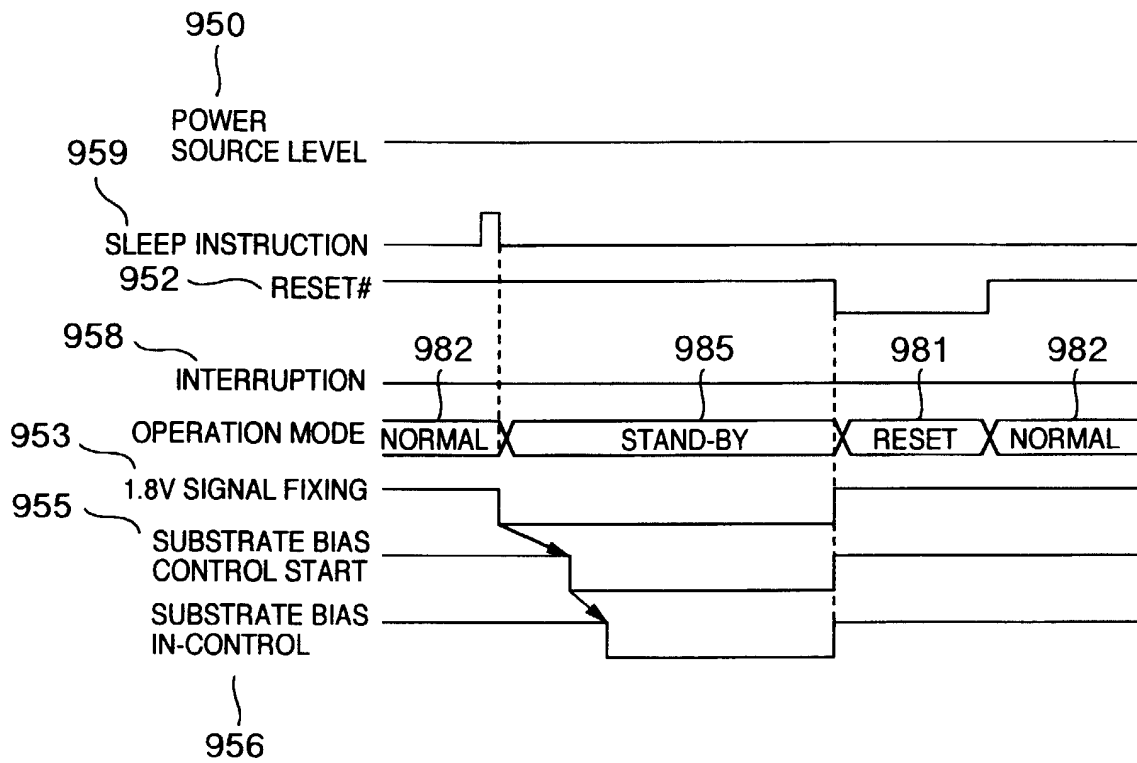
INTERNATIONAL SEARCH REPORT

	International application No.
	PCT/JP97/04253

A. CLASSIFICATION OF SUBJECT MATTER
Int. Cl^6 G06F1/04
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
Int. Cl^6 G06F1/04, H01L27/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926 - 1996	Jitsuyo Shinan Toroku
Kokai Jitsuyo Shinan Koho	1971 - 1997	Koho 1996 - 1998
Toroku Jitsuyo Shinan Koho	1994 - 1998	

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP, 7-254685, A (Toshiba Corp.), October 3, 1995 (03. 10. 95)(Family: none)	1, 16
A	JP, 8-83487, A (Mitsubishi Electric Corp.), March 26, 1996 (26. 03. 96)(Family: none)	1, 16
A	JP, 8-204140, A (NEC Corp.), August 9, 1996 (09. 08. 96)(Family: none)	1, 16

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search	Date of mailing of the international search report
February 17, 1998 (17. 02. 98)	March 3, 1998 (03. 03. 98)

Name and mailing address of the ISA/	Authorized officer
Japanese Patent Office	
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)